A 20W 2080-2200 MHz Hybrid Power Amplifier Optimized for Error Amplifier Applications

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Abstract **A hybrid power amplifier module has been designed for application as an error amplifier in feed-forward PAs for UMTS multi-channel operation. Error amplifiers require excess bandwidth, excellent gain flatness, and high linearity. Si LDMOS power devices were integrated with chip-and-wire matching and hybrid SMT amplifier circuitry chosen to optimize these characteristics.**

I. INTRODUCTION

Developments in the UMTS/IMT-2000 frequency band of 2.11 – 2.17 GHz are directed towards meeting the projected demand for broadband wireless services. Base station implementations typically support multiple channels of WCDMA protocol with feed-forward corrected power amplifier (PA) systems [1]. The total PA system includes several specialized amplifier circuits. These circuits can involve output stages capable of over 100 watts peak power, as well as preceding stages, including so-called driver stages. As total power capability has risen, the requirements of driver stages have also increased. High power amplifier designers place priority on design of the challenging output stages, and justifiably expect simpler driver stages to meet more stringent specifications. Essentially, drivers are expected to be "transparent" in their impact on power chains.

Perhaps the most demanding application for driver modules is as error amplifiers in feed-forward PAs. The error path of the PA is required to have excess bandwidth in order to achieve out-of-band correction (suppression of distortion products). Correction is diminished by any deviation from constant gain and linear phase in the error path. It is not uncommon to require a driver amplifier in the error path to possess double the bandwidth of the nominal communications band; gain flatness of tenths of a dB, and deviation from linear phase of less than one degree. There are also requirements for linearity (minimal distortion) over an extended dynamic range (typically 20 dB) as well as reduced power dissipation in backoff operation.

II. AMPLIFIER TOPOLOGY

Two amplifier topologies were considered in our development of power amplifier modules for the UMTS band: first, a single-ended stage followed by a quadrature balanced output stage; and second, two cascaded quadrature balanced stages.

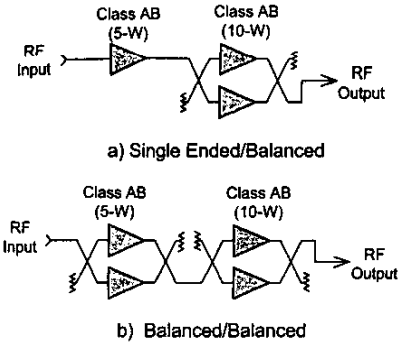

Figure 1. Alternative Amplifier Block Diagrams

The use of 3 dB quadrature couplers assures low stage VSWR[2], and therefore allows more independence in selection of the matching conditions presented to the transistors. This critical additional freedom supports optimization for gain flatness and linearity. In contrast, the single-ended input stage approach requires matching circuits that simultaneously optimize gain flatness, linearity, and input and output VSWR, with unavoidable tradeoffs. Therefore, the dual quadrature balanced stage approach is preferred for error amplifiers.

III. AMPLIFIER PARTITIONING – USE OF CHIP CARRIERS

Silicon LDMOS transistors were chosen as the active devices. These devices are widely applied in base stations because of their linearity in Class AB operation and established reliability and cost benefits. Because the output power requirement is limited for driver applications, the devices chosen were scaled down versions of existing 30-watt (26 cell) commercial devices. We chose to use 4-cell and 8-cell devices with nominal peak powers of 5 and 10 watts. Each transistor die is attached to a small metal chip carrier which is itself attached to a larger heat sink. The heat sink also serves as the base of the module. The base supports four chip carriers and an alumina amplifier substrate with matching circuitry realized using SMT components and transmission lines formed using thick-film metalization.

A critical issue in this design was the degree of matching to include on the chip carriers. It is well known that the most sensitive elements of matching

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circuits for LDMOS die are those elements in closest proximity to the die. Three possible approaches to on-chip-carrier matching are shown in Figure 2.

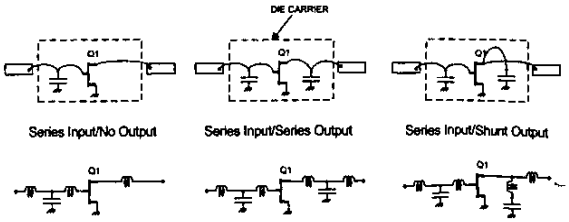

Figure 2. Alternatives for On-Chip-Carrier Matching

The shunt-output approach offers the widest bandwidth of these alternative topologies. This is illustrated by using a simple one-port model for the transistor output power matching conditions[3], estimated to be equivalent to a parallel combination of resistance and capacitance (typically 15 ohms and 12 picofarads, for these output LDMOS devices). The output matching provided by alternative circuit examples is given in Figure 3. The shunt output match approach provides the most promising impedance transformation to support wideband operation. Additionally, sensitivity to bond wire inductance and device capacitance variations is reduced somewhat with the shunt output approach.

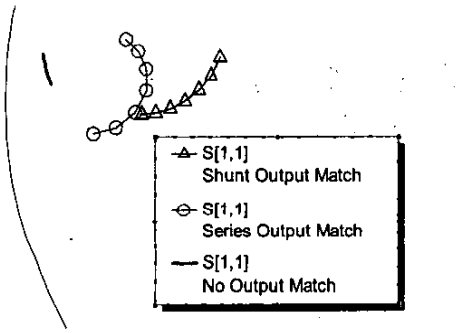

Figure 3. Examples of LDMOS Drain Matching Provided by the Alternative On-Chip-Carrier Circuits.

IV Matching Circuitry Synthesis & Optimization

The schematic of the dual stage amplifier module is shown in Figure 4. We chose to realize on-substrate matching circuits with a combination of distributed transmission line elements and lumped elements (chip SMT passive components). The 3 dB quadrature couplers are imbedded under the alumina substrate using inverted coplanar structures [4].

The choice of matching circuits was complicated by our limited ability to model all of the circuit influences and interactions under differing signal protocols. For example, the distortion products of two cascaded stages may be additive or may cancel to some degree. The first stage can potentially provide a degree of predistortion for the second stage.

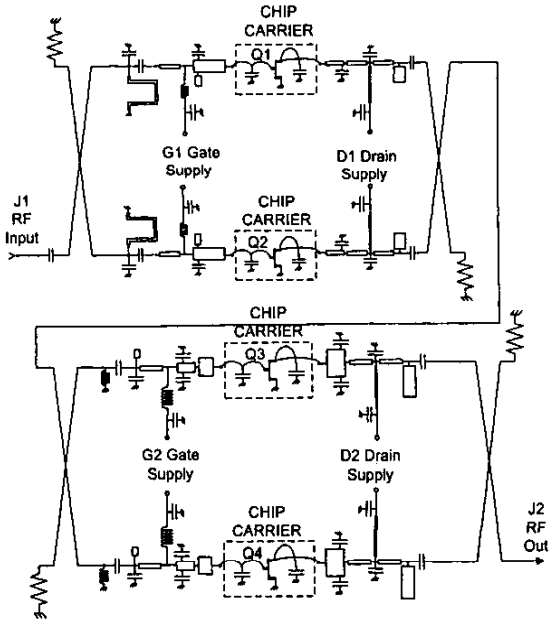

Figure 4. Two-Stage Amplifier Module Diagram

We chose to take a measurement-based approach to the circuit synthesis and optimization:

1. First, load-pull data was collected for each chip-carrier circuit for conditions of optimum output power. Chip carrier circuitry was iterated to produce the largest possible load contours.
2. Alumina substrate circuits were synthesized that provided tightly clustered matching impedances approximating the optimum load pull conditions over a wide bandwidth.
3. Matching circuits were required to have tuning elements that supported nominally orthogonal tuning (magnitude and angle of reflection coefficient) during logical empirical optimization.
4. Prototype circuits were measured using high-speed characterization test equipment that displayed, for example, 3rd, 5th, and 7th order IMDs versus output power as well as gain compression versus output power[5]. This allowed real time coupling of measurements, bias variation, and tuning.

Experience with tuning and testing in this manner demonstrated that intermodulation distortion levels were particularly sensitive to elements of the gate matching circuits, and to precise adjustment of quiescent bias levels of each stage.

V. Measurements

The two-stage amplifier gain was reduced (relative to turn-on values) in the process of tuning/optimization, as priority was placed on achieving minimum distortion and

minimum gain variation over frequency. This resulted in excellent gain flatness over a band that was double the nominal UMTS band (2110-2170 MHz), as demonstrated in Figure 5. Input and output return loss are less than –20 dB (1.22:1 VSWR). Phase linearity is (Figure 6) is less than ±0.2 degrees over 2110-2170 MHz and less than ±0.5 degrees over 2080 – 2200 MHz. Group delay is 3.5 nanoseconds.

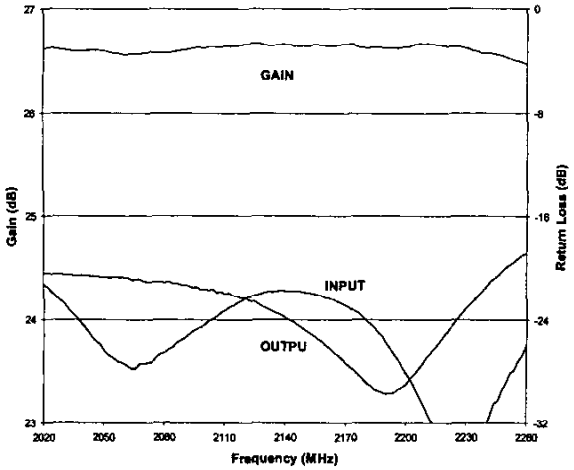

Figure 5. 2-Stage Module Gain & Return Loss versus Frequency (2020-2260 MHz, 30 MHz per division)

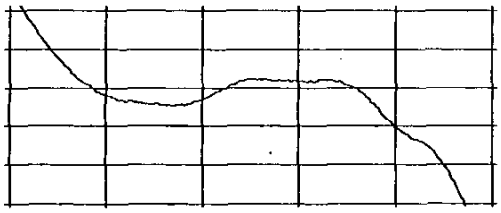

Figure 6. Module Deviation from Linear Phase (2 degrees/div, 1910 – 2310 MHz, 80 MHz, div.)

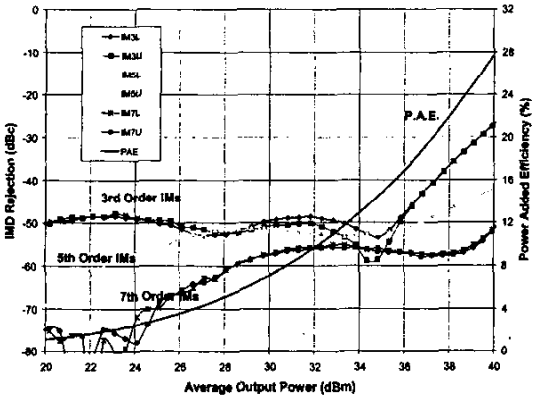

Figure 7. Two-Tone Intermodulation Distortion as a Function of Output Power (3rd, 5th, and 7th order, & PAE)

Although Class AB operation offers efficiency advantages over Class A operation, maintaining low distortion levels over an extended dynamic range is a challenge. Class AB operation normally produces distortion products with a distinct "hill" at lower power levels [6, 7], on the order of –35 to –45 dBc, which are influenced by bias conditions and source and load impedances. This can be exacerbated by additive contributions of multiple stages. It was determined that through proper matching conditions and differing quiescent bias conditions for the input and output stages, the amplifier could maintain 3rd order IMD levels below –45 dBc. Measured 3rd, 5th, and 7th order products are presented as a function of output level in Figure 7 (f=2140 MHz, Δf=931 KHz).

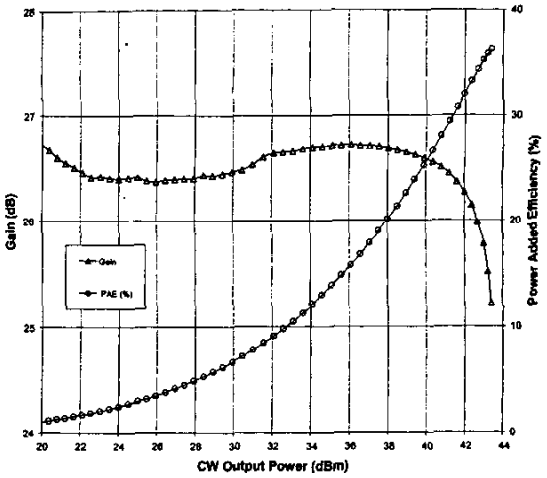

Figure 8. Gain & P.A.E. versus Output Power

Gain versus output power is presented in Figure 8. Output power at 1.0 dB gain compression is constant to within ±0.1 dBm over the primary band of 2110-2170 MHz, and to within ±0.2 dBm over the extended band of 2080-2200 MHz.

It is expected that this module will be used with a variety of signal protocols, including EDGE, WCDMA, CDMA, etc. For EDGE (Enhanced Data rate for GSM Evolution) applications, the standard performance criteria are EVM (error vector magnitude) and ACPR (Adjacent Channel Power Ratio). These are presented in figure 9. EVM is below 2.5% at an average output level of 8 W.

A primary measure of performance under WCDMA, adjacent channel power ratio, will vary depending on the particular signal characteristics. Peak-to-average levels from 7 to 12 dB are common. There appears to be a lack of consensus regarding stimuli used for amplifier characterization. In this case, a WCDMA source with an 8 dB peak-to-average was used. Adjacent channel power performance of the module is shown in Figure 10, measured per the 3GPP protocol.

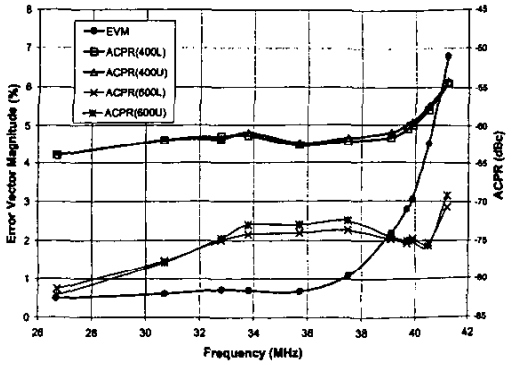

Figure 9. Module Performance under EDGE Protocol (Average Error Vector Magnitude and Adjacent Channel Power Ratio at 400 and 600 KHz offsets)

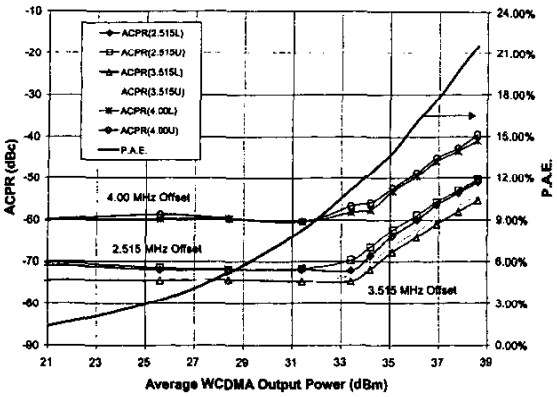

Figure 10 Module Performance with WCDMA Protocol (3GPP WCDMA with 8 dB peak-to-average. 1st ACPR @ 2.515 MHz & 30 KHz BW, 2nd ACPR @3.515 MHz & 30 KHz BW, 3rd ACPR @4.00 MHz & 1.0 MHz BW)

Specifications for performance of a drive amplifier will vary depending of the level of correction anticipated, and the linearity budget for elements of the feed-forward amplifier system.

The amplifier (Figure 11) was fabricated using standard thick film processing and construction [8]. The employment of a thick metal base and high thermal conductivity chip carriers resulted in a low thermal impedance of only 1.5 degrees C per watt total amplifier dissipation, at an output power level of 20 watts.

VI. Manufacturing Considerations

Tuning elements (generally small open stubs) have been identified during prototype test and alignment that provide for minute adjustment of gain flatness. Means of pre-testing and sorting chip-carrier assemblies, prior to amplifier assembly, are in development. Maintaining performance margins and product consistency are critical manufacturing objectives. Production data statistics will be presented at the Symposium.

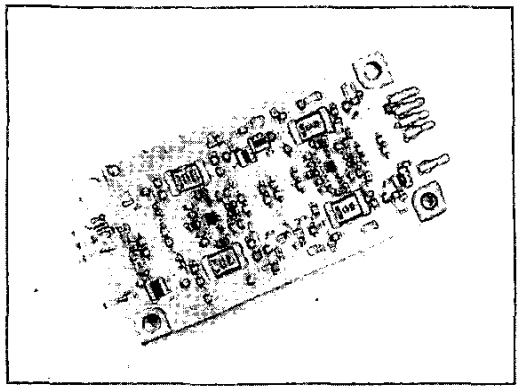

Figure 11 Two-Stage UMTS Driver Amplifier Module (Width is 1.25 inches. Length is 2.40 inches)

VI. Conclusion

A high performance UMTS driver amplifier module has been designed for application as an error amplifier in feed-forward PAs. Emphasis was on achieving excess bandwidth, tight gain flatness and phase linearity, and low distortion. Si LDMOS 5W & 10W devices were integrated with chip-and-wire matching on chip carriers, which were then inserted into hybrid thick-film circuitry with distributed and SMT matching elements. The resultant two-stage module achieves 26 dB gain, 20 Watts output, and 3rd order IMDs of –45 dBc over a 20 dB range of output power.

Acknowledgements

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